EE449 Analog Integrated Circuits Layout (Elective)

Course description:
Introduces the analog integrated circuit fabrication and layout design, or the analog VLSI. Lecture covers representative IC fabrication processes (standard bipolar, CMOS and analog BiCMOS), layout principles and methods of MOS transistors and device matching, resistors and capacitors layouts, the matched layouts of R and C, bipolar transistors and bipolar matching, and diodes. Lecture will also review several active-loaded analog amplifier circuits, including some CMOS and BiCMOS op amp configurations. Term project is required on layout design of simple Op Amp circuits involving CMOS or BiCMOS op amps plus several matched devices of resistors, capacitors and transistors. Circuits are designed using SPICE simulation. The layout design is verified by SPICE simulation of the net list extracted from the layout. The student term project is to be fabricated through MOSIS.

Prerequisite(s):
EE 311

Textbook(s):
Textbook: The Art of Analog Layout, A.Hastings, Prentice Hall (2001), ISBN 0-13-087061-7

Course objectives:
Understand the semiconductor fabrication technology; learn fabrication technologies and layout techniques for Resistors, Capacitors, MOS Transistors, Bipolar Transistors and Diodes to meet the circuit performance specification and device matching requirements. Design common-centroid layout techniques using various interdigitation patterns will be introduced in detail for matching multiple devices.

Topics covered:
Semiconductor Fabrication, Representative Processes, Failure Mechanism, MOS Transistor, Application of MOS Transistor and Matching, Resistor, Capacitor, Matching of Resistor and Capacitor, Bipolar Transistor, Application of Bipolar Transistor, and Diodes.

Class/laboratory schedule:
Tuesdays and Thursdays at 15:30 - 16:50

Professional Significance:
Students apply knowledge of currently available fabrication processes and their constraints and design devices and circuits on Si chip; Apply knowledge of analog layout rules and matching techniques and design the layout of transistor-matched analog Integrated Circuits; Analyze the circuit requirements, and lay out the designed analog integrated circuits for fabrication; and Conduct circuit simulation and verify the design based upon the extracted SPICE file from layouts.

Relationship of Course to Program Outcomes:

(a)	2	Much of materials properties and physics are the underlying knowledge for discussions of fabrication processes.
(b)	0	Course discusses statistical variation of device properties and how they are obtained.
(c)	2	Course mainly focuses on transistor and circuit design to meet design requirements

(d)	1	Term projects were performed in teams or individually.
(e)	1	Weekly and term projects require solving device and circuit problems.
(f)	0	
(g)	2	Written reports were required for the weekly assignments and the term project reports. Oral presentations were required for the final projects.
(h)	0	
(i)	2	Changing process generations, related design constrains, and design and simulation tools are implied throughout the course and thus the needs for lifelong-learning. Also used are software tools for (lifelong) learning.
(j)	2	Layout design rules closely follow the current Foundry process generations and related constraints. The need to employ industry-standard SPICE device models (BSIM3 or Level=8) versus currently employed model in the class (Level=3).
(k)	2	Design projects require using modern software tools for layout design and simulation (MAGIC and Spice3). Students need to use these tools fully for the course projects and assignments.
(ee1)	2	Semiconductor statistics; and statics in device parameter variations across wafer and across
(ee2)	2	Materials sciences and physics laws used in discussion of process physics.
(ee3)	0	
(ee4)	0	

Prepared by:
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